EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	12	(US-6816825-$ or US-6717576-$ or US-6538651-$ or US-6088716-$ or US-5966072-$ or US-6272650-$ or US-6173276-$ or US-6208345-$ or US-6006242-$ or US-5701400-$ or US-6324437-$ or US-6400996-$).did.	USPAT	OR	ON	2006/03/06 10:46
L5	127	((717/153).ccls.)	USPAT	OR	ON	2006/03/06 10:50
L6	127	((717/156).ccls.)	USPAT	OR	ON	2006/03/06 10:50
L7	3295	execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3	USPAT	OR	ON	2006/03/06 10:50
L8	1600	(execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3) and management	USPAT	OR	ON	2006/03/06 10:50
L9	1472	((execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3) and management) and software	USPAT	OR	ON	2006/03/06 10:50
L10	1394	(((execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3) and management) and software) and interface	USPAT	OR	ON	2006/03/06 10:50
L11	95	((((execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3) and management) and software) and interface) and (information near management near system)	USPAT	OR	ON	2006/03/06 10:50
L12	2	("6006242").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 10:50

EAST Search History

L13	33	(((((execut$4 and graph and parameter and time and input and output and control$3 and reference and compar$3 and external and result and modify$3) and management) and software) and interface) and (information near management near system)) and runtime	USPAT	OR	ON	2006/03/06 10:50
L14	127	((717/153).ccls.)	USPAT	OR	ON	2006/03/06 10:50
L15	127	((717/156).ccls.)	USPAT	OR	ON	2006/03/06 10:50
L16	184	((717/158).ccls.)	USPAT	OR	ON	2006/03/06 10:50
L17	283	((717/158).ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L18	165	((717/156).ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L19	0	(((717/156).ccls.)) and (((717/158).ccls.)) and (((717/153).ccls.)) and (runtime near parameter)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L20	0	(((717/156).ccls.)) and (((717/158).ccls.)) and (((717/153).ccls.)) and (runtime near execu$s)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L21	0	(((717/156).ccls.)) and (((717/158).ccls.)) and (((717/153).ccls.)) and (runtime near execu$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L22	1	(((717/156).ccls.)) and (((717/158).ccls.)) and (((717/153).ccls.)) and runtime and parameter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L23	0	(((717/156).ccls.)) and (((717/158).ccls.)) and (((717/153).ccls.)) and runtime and link	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50

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L24	163	((717/153).ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L25	2	("6006242").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 10:50
L26	471	execut$4 and graph and parameter and runtime and input and output and control$3 and compar$3 and result and modify$3	USPAT	OR	ON	2006/03/06 10:50
L27	353	L26 and @ad<= "20000728"	USPAT	OR	ON	2006/03/06 10:50
L28	23	L27 and (vertex or vertices)	USPAT	OR	ON	2006/03/06 10:50
L29	7	john near1 hayman	USPAT	OR	ON	2006/03/06 10:50
L30	10	john near1 hayman	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L31	0	joseph near1 skeffington near wholey	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L32	0	joseph near1 skeffington	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L33	0	brond near1 larson	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L34	28	craig near1 stanfill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L35	13	L34 and @ad <= "20000728"	USPAT	OR	ON	2006/03/06 10:50

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L36	0	joseph near1 skeffington	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L37	0	brond near1 larson	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L38	0	glenn near1 jhon	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L39	202	glenn near1 john	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L40	22	martin near2 serrano	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L41	0	glenn near1 allin	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L42	0	glenn near1 john near2 allin	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L43	0	glenn near2 john near2 allin	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50

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L44	28	craig near2 stanfill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L45	5	L40 and @ad <= "20000728"	USPAT	OR	ON	2006/03/06 10:50
L46	13	L44 and @ad <= "20000728"	USPAT	OR	ON	2006/03/06 10:50
L47	10	modify$5 adj5 graph and executable and vertices and links and (runtime or (run time))	USPAT	OR	ON	2006/03/06 10:50
L48	9	L47 and @ad <= "20000728"	USPAT	OR	ON	2006/03/06 10:50
L49	7	L48 and parameter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L50	20	modify$5 adj5 graph and executable and vertices and links and (runtime or (run time))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50
L51	9	L50 and @ad <= "20000728"	USPAT	OR	ON	2006/03/06 10:50
L52	7	L51 and parameter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 10:50

Terms used **Spice for Circuits and Electronics** Found **2,367** of **171,143**

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101 An efficient analytical model of coupled on-chip RLC interconnects
Liang Yin, Lei He
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Publisher: ACM Press
Full text available: pdf(165.29 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new decoupled model for two coupled transmission lines with consideration of the inductive effect. It maps two coupled lines into two completely isolated lines with separated drivers and receivers, and has no loss of accuracy during the decoupling procedure. Further, we derive a closed-form time domain response for an isolated transmission line using a one-segment RLC II model. Combining the two models, we have an analytical time-domain solution to two coupled tr ...

102 A static power model for architects
J. Adam Butts, Gurindar S. Sohi
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: ACM Press
Full text available: pdf(136.88 KB) ps(431.76 KB) Publisher Site Additional Information: full citation, references, citings, index terms

103 A framework for dynamic energy efficiency and temperature management
Michael Huang, Jose Renau, Seung-Moon Yoo, Josep Torrellas
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: ACM Press
Full text available: pdf(194.74 KB) ps(1.23 MB) Publisher Site Additional Information: full citation, references, citings, index terms

104 Session 9A: noise and performance issues in routing: Cross-talk immune VLSI design using a network of PLAs embedded in a regular layout fabric
Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on**

Computer-aided design
Publisher: IEEE Press
Full text available: pdf(150.21 KB) Additional Information: full citation, abstract, references, citings

We present a VLSI design methodology to address the cross-talk problem, which is becoming increasingly important in Deep Sub-Micron (DSM) IC design. In our approach, we implement the logic netlist in the form of a network of medium sized PLAs. We utilize two regular layout "fabrics" in our methodology, one for areas where PLA logic is implemented, and another for routing regions between such logic blocks. We show that a single PLA implemented in the first fabric style is not only cross-talk immu ...

105 Session 8A: static timing analysis: Slope propagation in static timing analysis
David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Chanhee Oh, Rajendran Panda
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(116.13 KB) Additional Information: full citation, abstract, references, citings

Static timing analysis has traditionally used the PERT method for identifying the critical path of a digital circuit. Due to the influence of the slope of a signal at a particular node on the subsequent path delay, an earlier signal with a signal slope greater than the slope of the later signal may result in a greater delay. Therefore, the traditional method for timing analysis may identify the incorrect critical path and report an optimistic delay for the circuit. We show that the circuit delay ...

106 Energy-efficient 32 × 32-bit multiplier in tunable near-zero threshold CMOS
Vjekoslav Svilan, Masataka Matsui, James B. Burr
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(446.48 KB) Additional Information: full citation, abstract, references, citings, index terms

An 80,000 transistor, low swing, 32~x~32-bit multiplier was fabricated in a standard 0.35&mgr;m,Vth=0.5 V CMOS process and in a 0.35&mgr;m, back-bias tunable, near-zero Vth process. While standard CMOS atVdd=3.3 V runs at 136 MHz, the same performance can be achieved in the low- Vth version at Vdd=1.3 V, ...

107 A low-voltage CMOS multiplier for RF applications (poster session)
Carl James Debono, Franco Maloberti, Joseph Micallef
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(235.14 KB) Additional Information: full citation, abstract, references, citings, index terms

A low-voltage analog multiplier operating at 1.2V is presented. The multiplier core consists of four MOS transistors operating in the saturation region. The circuit exploits the quadratic relation between current and voltage of the MOS transistor in saturation. The circuit was designed using standard 0.6&mgr;m CMOS technology. Simulation results indicate an IP3 of 4.9dBm and a spur free dynamic range of 45dB.

Keywords: CMOS, RF, analog multiplier, low-voltage

108 Low power mixed analog-digital signal processing
Mattias Duppils, Christer Svensson
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(376.94 KB) Additional Information: full citation, abstract, references, index terms

The power consumption of mixed-signal systems featured by an analog front-end, a digital back-end, and with signal processing tasks that can be computed with multiplications and accumulaðtions, is analyzed. An implementation is proposed, composed of switched-capacitor mixed analog/digital multiply accumulate units in the analog front-end, followed by an A/D converter. This impleðmentation is shown to be superior in respect of power consumption compared to an equivalent implementation with a ...

109 A three-port nRERL register file for ultra-low-energy applications

Jun-Ho Kwon, Joonho Lim, Soo-Ik Chae

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(1.86 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we propose an adiabatic register file for ultra-low-energy applications, which uses a new reversible adiabatic logic, nRERL [1]. The nRERL register file discards garbage information with minimal energy dissipation. We designed a 16x8b three-port nRERL register file. From SPICE simulations, we found that the nRERL register file consumes less than 10% of the energy consumed in the conventional register file at the frequency of lower than 1MHz. We also describe ...

110 New clock-gating techniques for low-power flip-flops

A. G. M. Strollo, E. Napoli, D. De Caro

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(838.28 KB) Additional Information: full citation, abstract, references, citings, index terms

Two novel low power flip-flops are presented in the paper. Proposed flip-flops use new gating techniques that reduce power dissipation deactivating the clock signal. Presented circuits overcome the clock duty-cycle limitation of previously reported gated flip-flops.Circuit simulations with the inclusion of parasitics show that sensible power dissipation reduction is possible if input signal has reduced switching activity. A 16-bit counter is presented as a simple low power applic ...

Keywords: CMOS digital integrated circuits, flip-fops, low-power circuits, transition probability

111 Wave-steering one-hot encoded FSMs

Luca Macchiarulo, Malgorzata Marek-Sadowska

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(90.59 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we address the problem of pipelining FSMs by extending wave-steering scheme from combinational to sequential realm. A unified approach employs direct mapping of State Transition Graph into a circuit realization. Experimental result on MCNC benchmarks show performance improvement of 2 to 4 times at the cost of an average area increase of 2.9 times.

112 Cost based tradeoff analysis of standard cell designs

Peng Li, Pranab K. Nag, Wojciech Maly

April 2000 **Proceedings of the 2000 international workshop on System-level interconnect prediction**

Publisher: ACM Press

Full text available: pdf(318.11 KB) Additional Information: full citation, references, citings, index terms

Keywords: a posteriori wire length estimation, die size estimation, yield and cost prediction

113 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

114 Noise estimation due to signal activity for capacitively coupled CMOS logic gates

Kevin T. Tang, Eby G. Friedman

March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Publisher: ACM Press

Full text available: pdf(630.94 KB) Additional Information: full citation, abstract, references, index terms

The effect of interconnect coupling capacitance on neighboring CMOS logic gates driving coupled interconnections strongly depends upon the signal activity. A transient analysis of two capacitively coupled CMOS logic gates is presented in this paper for different combinations of signal activity. The uncertainty of the effective load capacitance and propagation delay due to the signal activity is addressed. Analytical expressions characterizing the output voltage and propagation delay are also ...

115 A 12b 50 MHz 3.3V CMOS acquisition time minimized A/D converter

Young-Deuk Jeon, Byeong-Lyeol Jean, Seung-Chul Lee, Sang-Min Yoo, Seung-Hoon Lee

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(125.13 KB) Additional Information: full citation, references

116 Analysis of power-clocked CMOS with application to the design of energy-recovery circuits

Massoud Pedram, Xunwei Wu

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(114.01 KB) Additional Information: full citation, references

117 A benchmark suite for substrate analysis

Edoardo Charbon, Luis Miguel Silveira, Paolo Miliozzi

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(253.99 KB) Additional Information: full citation, references

118 Static timing analysis taking crosstalk into account

Mattias Ringe, Thomas Lindenkreuz, Erich Barke
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: ACM Press
Full text available: pdf(62.37 KB) Publisher Site
Additional Information: full citation, references, citings, index terms

119 A new approach for computation of timing jitter in phase locked loops

M. M. Gourary, S. G. Rusakov, S. L. Ulyanov, M. M. Zharov, K. K. Gullapalli, B. J. Mulvaney
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: ACM Press
Full text available: pdf(55.58 KB) Publisher Site
Additional Information: full citation, references, index terms

120 Analytical macromodeling for high-level power estimation

Guiseppe Bernacchia, Marios C. Papaefthymiou
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(93.34 KB)
Additional Information: full citation, abstract, references, citings, index terms

This paper present a new macromodeling technique for high-level power estimation. Our technique is based on a parameterizable analytical model that relies exclusively on statistical information of the circuit's primary inputs. During estimation, the statistics of the required metrics are extracted from the input stream, and a power estimate is obtained by evaluating a model function that has been characterized in advance. Our model yields power estimates within seconds, because it does not ...

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